

Appln No.: 09/662,054

Applicant(s): Randy Bonella et al.
DIGITAL SYSTEM OF ADJUSTING DELAYS ON CIRCUIT

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**BOARDS** 

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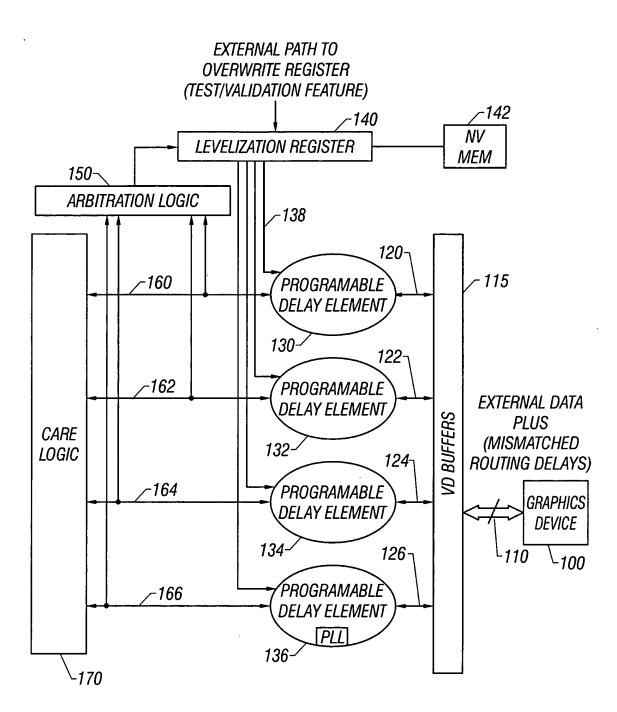


FIG. 1



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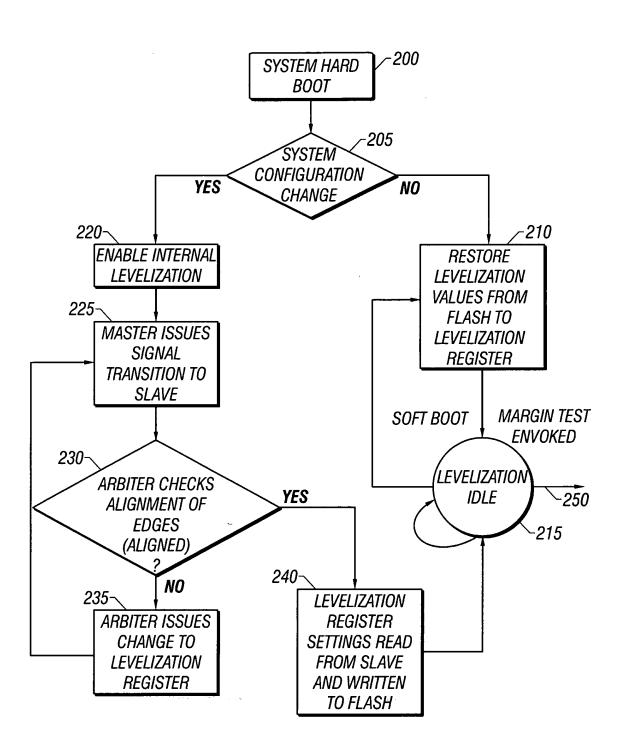


FIG. 2



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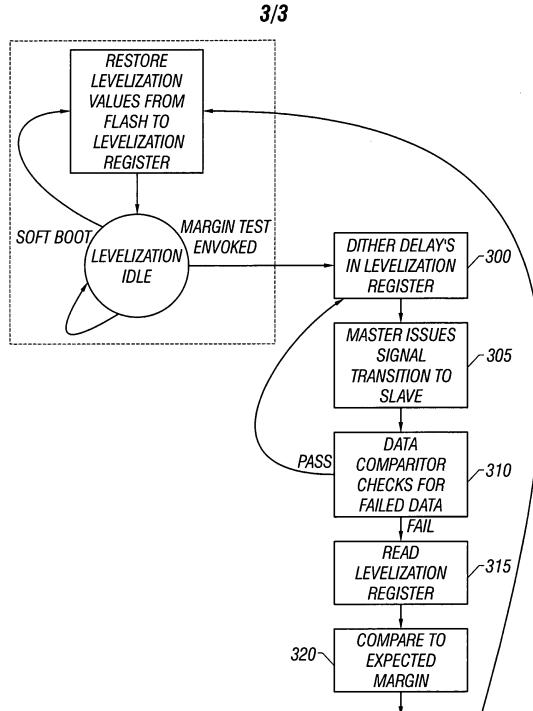


FIG. 3

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**ISSUE VALIDATION** 

REPORT AND RESTORE SYSTEM